REMARKS

Claims 1-31 are pending in the present application. Claims 1, 21 and 23 are independent claims. Claims 1, 21 and 23 are amended by this Reply. Reconsideration of this application, as amended, is respectfully requested.

REJECTIONS UNDER 35 U.S.C. §102

Claims 1, 7-10, 13, 16-18, 21-23 and 27-31 stand rejected under 35 U.S.C. §102(e) over U.S. Patent No. 5,982,467 to Lee, for the reasons set forth in paragraph 1 of the Office Action. This rejection is respectfully traversed.

In the Examiner's responses to Applicants' only arguments, the Examiner asserts that with regard to claim 1, Lee discloses (Fig.D) a metallic pattern forming a drain electrode 137 of the thin film transistor and a storage electrode 119 of the storage capacitor, and admits that the drain electrodes and storage electrodes are not a single layer and do not share a common layer. With regard to claim 23, the Examiner admits that the drain electrodes and storage electrodes of Lee are not a single layer and do not share a common layer. While admitting that these distinctions exist, the Examiner states that claims 1 and 23 fail to disclose that the storage electrodes and drain electrodes share a common point or metallic pattern with a continuous layer (claim 21 is similar).

While not conceding the appropriateness of the Examiner's rejection, but merely to advance prosecution of the instant application, Applicants respectfully submit that independent claim 1 has been amended to recite a combination of

elements in a liquid crystal device having a thin film transistor including a metallic pattern including a drain electrode of the thin film transistor and a storage electrode of the storage capacitor in a single layer, claim 21 has been amended to recite a combination of elements in a liquid crystal device having a thin film transistor including a storage capacitor including a storage electrode and a drain electrode in a single layer and claim 23 has been amended to recite a combination of elements in a method of manufacturing a thin film transistor substrate including forming a semiconductor layer over at least a portion of one of the gate electrodes, at least a portion of one of the source electrode, and at least a portion of the drain electrode part in a single layer.

Applicants respectfully submit that this combination of elements as set forth in independent claims 1, 21 and 23 is not disclosed or made obvious by the prior art of record, including Lee.

With regard to dependent claims 7-10, 13, 16-18, 22 and 27-31, Applicants submit that claims 7-10, 13, 16-18, 22 and 27-31 depend, either directly or indirectly, from independent claims 1, 21 and 23 which are allowable for the reasons set forth above, and therefore claims 7-10, 13, 16-18, 22 and 27-31 are allowable based on their dependence from claims 1, 21 and 23. Reconsideration and allowance thereof are respectfully requested.

REJECTIONS UNDER 35 U.S.C. §103

Claims 2 and 24 stand rejected under 35 U.S.C. §103(a) over Lee as applied

to claims 1 and 23 above, and further in view of U.S. Patent No. 6,100,953A to Kim et al. (Kim). This rejection is respectfully traversed.

The Examiner asserts that Kim discloses a metallic pattern having a drain electrode of a thin film transistor and a storage electrode wherein the metallic pattern is spaced a predetermined distance from the data line.

Kim, however, like Lee (argued above with respect to claims 1, 21 and 23), does not disclose or suggest a metallic pattern including a drain electrode of the thin film transistor and a storage electrode of the storage capacitor in a single layer, as recited in independent claim 1 (as amended) and similarly stated in independent claims 21 and 23 (as amended).

Claims 2 and 24 depend on claims 1 and 23, either directly or indirectly. Therefore Lee, in view of Kim, cannot render claims 2 and 24 obvious to one of ordinary skill in the art. Accordingly, reconsideration and withdrawal of this art grounds of rejection are respectfully requested.

ALLOWABLE SUBJECT MATTER

The Applicants appreciate the Examiner's indication that claims 3-6, 11, 12, 14, 15, 19, 20, 25 and 26 contain allowable subject matter, and would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Claims 3-6, 11, 12, 14, 15, 19, 10, 25 and 26 have not been rewritten at this time, because it is believed that claims 1, 21 and 23, from which these claims depend, are allowable.

CONCLUSION

Applicants point out that all of the Examiner's comments have been addressed and that all of the Examiner's objections and rejections have been overcome, thereby placing all claims pending in the present Application in condition for allowance. Allowance of the claims is respectfully solicited.

In the event that any outstanding matters remain in this application, Applicants request that the Examiner contact Percy L. Square at (703) 205-8034 to discuss such matters.

Attached hereto is a marked-up version of the changes made to the application by this Amendment.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

Respectfully submitted,

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Attachment: Version with Markings to Show Changes Made

(Rev. 02/06/01)

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

The claims have been amended as follows:

1. (Twice Amended) A liquid crystal device having a thin film transistor, comprising:

a plurality of gate lines formed on a substrate;

a plurality of data lines insulated from and intersecting said gate lines, said data lines and intersecting gate lines defining a plurality of cells, at least one cell including,

a pixel electrode,

a thin film transistor connected to one of the data lines and one of the gate lines defining the cell,

a storage capacitor, and

a metallic pattern [forming] including a drain electrode of the thin film transistor and a storage electrode of the storage capacitor in a single layer, and being electrically connected to the pixel electrode.

21. (Three Times Amended) A liquid crystal device having a thin film transistor, comprising:

a plurality of gate lines formed on a substrate;

a plurality of data lines insulated from and intersecting said gate lines, said data lines and intersecting gate lines defining a plurality of cells, at least one cell including,

a pixel electrode,

a thin film transistor interposed between one of the data lines and the pixel electrode and including a source electrode connected to the one of the

data lines, a gate electrode connected to one of the gate lines, a drain electrode, and

a storage capacitor [having] including a storage electrode and a drain electrode in a single layer, the storage capacitor being connected to the pixel electrode.

23. (Twice amended) A method of manufacturing a thin film transistor substrate, comprising:

forming a gate line having a gate electrode on a transparent substrate;

forming a gate insulating layer on the gate electrode;

forming a semiconductor layer on the gate insulating layer;

forming a data line having a source electrode, and a metallic pattern [having] including a drain electrode part and a storage electrode part;

forming a semiconductor layer over at least a portion of one of the gate electrodes, at least a portion of one of the source electrode, and at least a portion of the drain electrode part in a single layer;

forming a protective film over the entire surface; and

forming a pixel electrode over the protective film.